Interfacing the LTC1091 to the COP820C MCU

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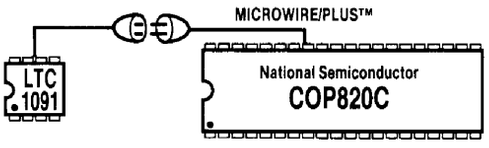


Introduction

This application note describes the hardware and software required for communication between the LTC1091 10-bit data acquisition system and the National Semiconductor COP800 microcontroller family which uses the MICROWIRE/PLUS serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 45μs. Configuration of the LTC1091 and the COP820C will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1091 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a half duplex, synchronous, format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE/PLUS is a synchronous, full duplex, serial port built into the COP800 family that allows easy interface to the LTC1091. MICROWIRE/PLUS provides clock, data in and data out lines that are compatible with the LTC1091. One additional line (G1) is required to control the $\overline{CS}$ pin on the LTC1091. The schematic of Figure 1 shows how the two devices are connected.

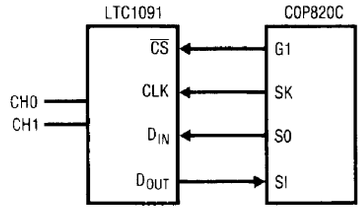


Figure 1. Schematic

Hardware Description

The actual interface was done using the COP820C, a member of the COP800 family. All code shown here should work with any of the COP800 family.

The code for this interface was developed on a COP820 evaluation board operated in the emulation mode.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer. A 5MHz COP820C clock (2μs instruction cycle) was used. By operating the MCU with a 1μs instruction cycle (high speed option) the minimum conversion and transfer time of 45μs is achieved.

The analog section of the schematic in Figure 1 is omitted for clarity. for a complete discussion of the analog considerations involved in using the LTC1091 please see the data sheet.

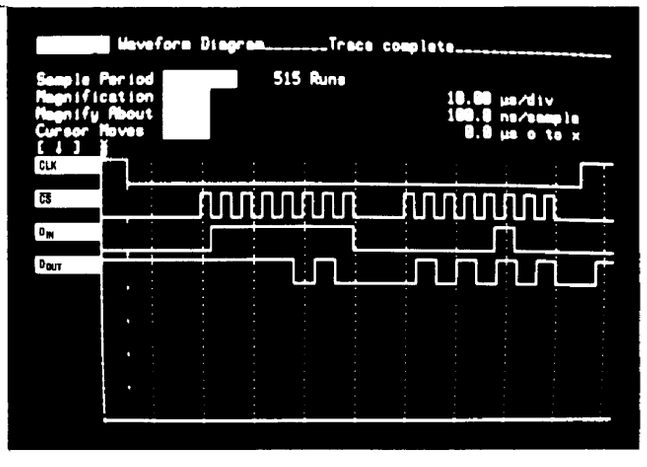


Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE/PLUS serial interface of the COP820C. Additionally, the software manipulates G1 ($\overline{CS}$ of the LTC1091).

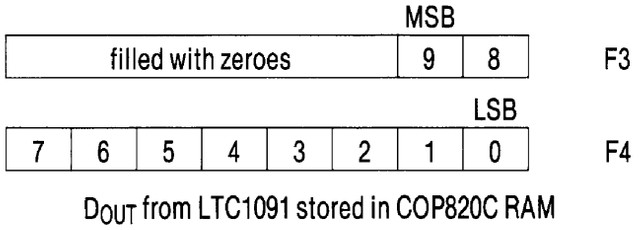
The code first loads the D_{IN} word of the LTC1091 into the memory address $F0. The D_{IN} word ($7F) contains a leading zero which is ignored, followed by a start bit. The next two bits configure the LTC1091 for CH1 with respect to ground. The fifth bit configures the A/D for MSB first mode and the remaining three LSBs are ignored as shown in Figure 3.

Next port G is configured such that pin G1 is an output and the MICROWIRE/PLUS serial port is a master. The control register is configured to enable SO and SK. Also the SK divide by is set up in such a way that the SK clock rate is equal to the crystal frequency divided by 20. The address of the port G data register is put into the B register so that the individual bits of port G can be manipulated. G1 ($\overline{CS}$) is then initialized by setting it high.

The D_{IN} word is then loaded into the accumulator. G1 is cleared and the LTC1091 D_{IN} word is loaded into the MICROWIRE™ shift register. The busy bit is set which begins the data transfer. 16 NOPs are used as a timer to allow the transfer to be completed. After the transfer is complete the D_{OUT} information is loaded into the accumulator and the next eight bits start to shift. The six MSBs in the accumulator are set to zeroes and the result is stored in $F3. Nine NOPs are then used to wait until the second eight bits have been shifted. G1 ($\overline{CS}$) is then set and the

0	1	1	1	1	1	1	1
Ignore	Start	S/D	O/S	MSBF	don't care	don't care	don't care

Figure 3. 4-Bit D_{IN} Word for LTC1091 in $F0



D_{OUT} from LTC1091 stored in COP820C RAM

Figure 4. Memory Map

LABEL	MNEMONIC	COMMENTS
	LD (F0)←$7F	LOAD D_{IN} WORD INTO $F0
	LD (D5)←$32	G1 IS OUT, MICROWIRE MASTER
	LD (EE)←$08	ENABLE SO, SK
	LD (B)←$D4	PORT G DATA ADDR INTO B
	SBIT 1	G1 SET (CS GOES HIGH)
LOOP	LD (A)←(F0)	PUT LTC1091 D_{IN} WORD IN ACC
	RBIT 1	G1 CLEARED (CS GOES LOW)
	X (A)←→(E9)	D_{IN} IN MICROWIRE SHIFT REG.
	LD (B)←$EF	PUT PSW REG. ADDR. INTO B
	SBIT 2	BUSY BIT SET TRANSFER START
	NOP	16 NOPs FOR TIMING
	X (A)←→(E9)	LOAD D_{OUT} INTO ACC
	SBIT 2	BUSY BIT SET TRANSFER START
	AND #03	MASK OUT UNUSED BITS
	X (A)←→(F3)	LOAD D_{OUT} INTO ADDR F3
	NOP	
	LD (B)←$D4	PORT G DATA REG. ADDR. IN B
	SBIT 1	G1 SET (CS GOES HIGH)
	X (A)←→(E9)	LOAD D_{OUT} INTO ACC
	X (A)←→(F4)	LOAD LSB INTO ADDR. F4

Figure 5. Code

data is loaded into the accumulator. The LSBs are then loaded into memory location $F4. The data at this point is right justified. With the appropriate shift routine the data can be easily left justified.

Summary

A four wire interface between the LTC1091 and the COP820C with a combined data conversion and transfer time of 45μs was demonstrated. The interface used the MICROWIRE/PLUS serial port of the COP820C. The 10 data bits of the LTC1091 are shifted MSB first in two eight bit transfers. The data is stored right justified in the COP820C's internal RAM.

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